Remarks

Reconsideration as well as allowance of the above-identified application, as currently amended, is respectfully requested.

By the above-made amendments, independent claim 20 is being amended to structurally highlight that both the drain and source of the p-channel load MISFETs of the respective SRAM cells of the semiconductor integrated circuit device set forth in independent claim 20 and, therefore, also according to the corresponding dependent claims thereof, are formed inside the semiconductor substrate, consistent with that shown in the example embodiments of Figs. 9, 11 and 16 of the drawings, etc., although not limited thereto.

The invention according to claim 20 is a semiconductor integrated circuit device comprising a semiconductor substrate; and a plurality of SRAM cells disposed on the semiconductor substrate, each having a pair of n-channel drive MISFETs, a pair of p-channel load MISFETs and a pair of n-channel selection MISFETs, wherein both the n-channel drive MISFETs and n-channel selection MISFETs are characterized by a LDD structure, each of the p-channel load MISFETs has a source, a drain and a gate electrode in which both the drain and source thereof are formed inside the semiconductor substrate, and the p-channel load MISFETs contain a single drain structure, respectively.

Regarding claim 21 (dependent on claim 20) an example construction thereof would include a 6-MIS type memory cell configuration or a complete CMIS (complementary metal insulator semiconductor) type memory cell, in which the drive and load MISFETs are configured as a pair of CMIS inverter circuits, in which the load MISFETs are p-channel type and in which both the drain and source of each are formed inside (within) the semiconductor substrate (e.g., Figs. 9, 11, 16, etc.). Regarding claim 21 (dependent on claim 20) the invention is further characterized by a [cross-connected]

two inverter circuit construction associated with each SRAM cell. Claim 22 (dependent on claim 20) further details the LDD structure associate with the n-channel drive MISFETs and n-channel selection MISFETs of the respective SRAM cells. Claim 23 (dependent on claim 20) further limits the substrate to one comprised of a single crystal silicon layer in which the drain of the p-channel load MISFETs are formed therein, respectively, and claim 24 (also dependent on claim 20) further characterizes the semiconductor IC device to a construction in which the drain is positioned under the gate electrodes thereof.

It is submitted, the invention according to independent claim 20 as well as the corresponding dependent claims thereof, as currently amended, was neither disclosed nor suggested by Ikeda, et al. (U.S. Patent No. 4,898,148). Therefore, the outstanding rejection, insofar as presently applicable, is traversed and withdrawal of the same is respectively requested. It is emphasized, independent claim 20 is considered, also, a generic claim to claims 23 and 24 which depend therefrom. Accordingly, examination as well as favorable action of claims 23 and 24 is also respectfully requested.

Ikeda, et al.'s ('148) SRAM cell construction features resistance cell elements (e.g., R_1, R_2) that are formed above the semiconductor substrate surface. For example, Ikeda, et al. calls for the formation of polysilicon resistances as the resistance load elements of the SRAM cells. For example, as can be see from Figs. 3 and 10 in Ikeda, et al., the load resistances R_1, R_2 of the SRAM cell are formed from a polycrystalline silicon layer 14 (14B) which is formed on an insulator film 12. (Column 8, lines 45 – 56, in Ikeda, et al. '148.) That is the load resistances R_1, R_2 in Ikeda, et al. are formed from a polycrystalline silicon material insulatedly above the semiconductor substrate, in clear contradistinction with that according to independent claim 20, as now amended, and further according to the corresponding dependent claims thereof. It is also noted that one end of each of the load resistances R_1, R_2, in Ikeda, et al., is connected to a power source potential wiring (e.g., 14A, V_{cc}). (Column 9, lines 11 – 29, in Ikeda, et al.)

In independent claim 20 of Applicants invention, the device construction sets forth a scheme in which, also, the drain as well as the source of each of the p-channel load MISFETs of the respective SRAM cells are formed inside the semiconductor substrate. Such, it is submitted, was neither disclosed and is contrary to that even suggested by Ikeda, et al. In this respect, while the present invention calls for, among the various set forth aspects thereof, the active regions of the p-channel load MISFETs to be formed inside (within) the semiconductor substrate, Ikeda, et al.'s scheme teaches a vertical arrangement in which the load elements are in the form of polycrystalline silicon resistances insulatedly stacked above the semiconductor substrate. For the same similar reason therefore, the invention according to claims 21 and 22, both of which depend from claim 20, are likewise defining over the teachings of Ikeda, et al. Moreover, since claims 23 and 24 are also dependent on claim 20 and since the latter is a genus claim to claims 23 and 24, examination as well as favorable action regarding withdrawn claims 23 and 24 for the same and similar reasons as that discussed above is also respectively requested.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration as well as withdrawal of the outstanding rejection and early allowance above-identified application is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned representative at the telephone number indicated below.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout

& Kraus, LLP, Dep. Acct. No. 01-2135 (1374.40147CX2), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Larry N. Anagnos
Reg. No. 32,392

LNA/gjb
(703) 312-6600